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### Method and apparatus for the automatic correction of faulty wires ...

The logic **simulation** hardware **emulator** of claim 5, wherein the **spare** select .... Upon detection of a **fault** on a regular **signal wire**, the runtime control ...

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1 illustrates a **fault simulation** system, according to an embodiment of the invention; [0014] FIG. 2 illustrates a front panel of a **signal** generator, ...

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tern Generation (ATPG) or **fault simulation**, which are. computationally expensive tasks for ... **signal** paths. Similarly, for interconnect test, the **wires** ...

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**faults** by creating a "faulty" PUT longer than the other "**fault-free**" ...  
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